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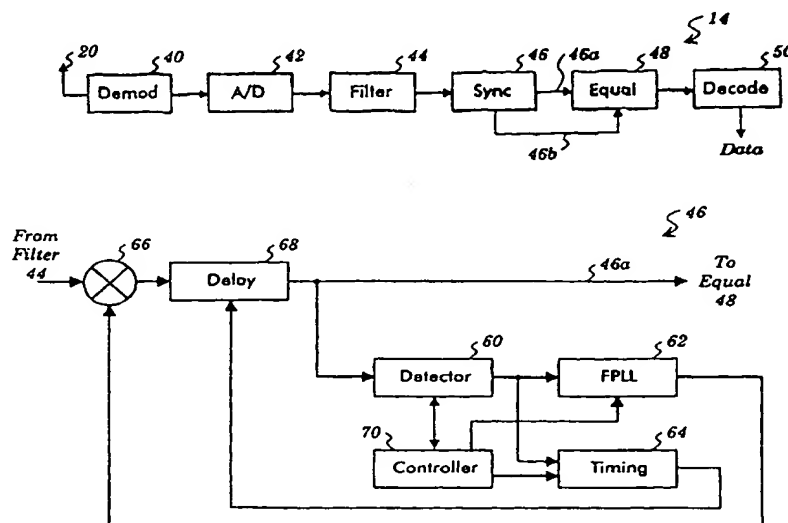
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(54) Title: RECEIVER SYNCHRONIZER USING CHIRPS SEQUENCES



(57) Abstract

A receiver receives a received signal containing a pilot up chirp and a pilot down chirp. The pilot up chirp has a frequency which increases from a time reference zero to a time reference t_N , and the pilot down chirp has a frequency which decreases from the time reference t_N to a time reference $2t_N$. A sampler of the receiver is arranged to sample the received signal. A detector is arranged to correlate the received signal samples with a reference up chirp and a reference down chirp. The reference up chirp has a varying frequency substantially matching the pilot up chirp, and the reference down chirp has a varying frequency substantially matching the pilot down chirp. A sample adjuster is arranged to synchronize the received signal samples in response to the detector.

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RECEIVER SYNCHRONIZER USING CHIRPS SEQUENCES

Technical Field of the Invention

5 The present invention relates to a synchronizer for a receiver and, more particularly, to a synchronizer that synchronizes a receiver to a received signal.

Background of the Invention

10 Data communication systems typically involve a transmitter, a receiver, and a communication path between the transmitter and receiver. The transmission path may be air or cables (wire or optical fiber). Although the present invention may be used in many different data communication system applications, it is described herein in the context of a cable system. However, it should be
15 understood that the cable system environment is merely an exemplary environment for the present invention and that the present invention may be used in many other environments.

 A cable system typically includes a head end which transmits data to a plurality of subscribers over a cable network. Typically, the cable network is at
20 least partially buried and has a main trunk carrying data directly from the head end, branch lines branching out of the main trunk, and subscriber lines carrying data between the branch lines and the subscribers. Considerable labor is required in running the subscriber lines from the branch lines to subscribers, particularly for those subscribers who are located at distances such as 1,000 feet or more from the
25 branch lines.

 Instead of running subscriber lines from branch lines to subscribers, transmitters could be located periodically along the branch lines in order to transmit data over the air between branch lines and subscribers. Thus, the substantial labor which is necessary to connect a subscriber to a branch line is materially reduced.

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However, care must be exercised in locating such transmitters. For example, if a subscriber is covered by only one transmitter, there may be areas within the premises of the subscriber where reception is poor.

The possibility of poor reception can be lessened by locating the transmitters so that the premises of each subscriber is covered by two or more transmitters. Unfortunately, because each transmitter operates at the same carrier frequency, and because of the variable distances between a subscriber's premises and the transmitters that cover the subscriber's premises, the same data may arrive at a reception site within a subscriber's premises at different times and with different phases. As a result, interference, referred to herein as ghosting, is produced.

If signal amplitude versus frequency of the received signal at a reception site in a subscriber's premises covered by two transmitters is graphed, an interference pattern can result. In the case where the reception site is located at an equal distance from both transmitters, the resulting interference pattern is characterized by periodic, sharply defined nulls at which the received signal is substantially undetectable, particularly in the presence of noise. That is, noise in the channel establishes a signal detection threshold such that any frequency components of the transmitted signal near or at the nulls will be difficult or impossible to detect because the signal to noise ratio at these points is too low. Moreover, when the received signal is processed through an equalizer, the signal to noise ratio can worsen, making signal detection even more difficult.

It is known how to adequately receive signals in the presence of white noise. For example, trellis encoding and Viterbi decoding may be used to encode and decode transmitted data adequately when white noise is present, because this type of coding and decoding performs well under white noise conditions. Unfortunately, trellis encoding and Viterbi decoding do not work particularly well in the presence of non-randomly distributed noise, such as may be present in an environment experiencing the above described interference pattern.

However, as disclosed in co-pending U.S. Patent Application Serial No. (DF-7005), data may be transmitted as code vectors which may be decoded in

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the receiver in such a way as to lessen the effect of non-randomly distributed noise on the recovery of the data from the transmitted signal. When code vectors are used to transmit data, the receiver must be synchronized to the received signal so that the transmitted code vectors can be accurately recovered and decoded. Prior
5 synchronization arrangements are not useful and/or efficient for the accurate recovery and decoding of transmitted code vectors.

The present invention is arranged to overcome one or more of the above-stated problems.

10 Summary of the Invention

According to one aspect of the present invention, a receiver receives a received signal containing a pilot up chirp and a pilot down chirp. The receiver comprises a detector and a signal adjuster. The detector is arranged to correlate the received signal with a reference up chirp and a reference down chirp. The
15 reference up chirp corresponds to the pilot up chirp, and the reference down chirp corresponds to the pilot down chirp. The signal adjuster is arranged to synchronize the receiver to the received signal in response to the correlation performed by the detector.

According to another aspect of the present invention, a receiver
20 receives a received signal containing a pilot up chirp and a pilot down chirp. The pilot up chirp has a frequency that increases from a time reference zero to a time reference t_N , and the pilot down chirp has a frequency that decreases from the time reference t_N to a time reference $2t_N$. The receiver comprises a detector and a signal adjuster. The detector is arranged to correlate the received signal with a reference
25 up chirp and a reference down chirp. The reference up chirp has a frequency substantially matching the pilot up chirp, and the reference down chirp has a frequency substantially matching the pilot down chirp. The signal adjuster is arranged to synchronize the receiver to the received signal in response to the correlation performed by the detector.

30 According to yet another aspect of the present invention, a method is provided for synchronizing a receiver to a received signal. The received signal

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contains a pilot up chirp and a pilot down chirp. The pilot up chirp has an increasing frequency, and the pilot down chirp has a decreasing frequency. The method comprises the following steps: a) correlating the received signal with a reference up chirp and a reference down chirp to produce a maximum up correlation and a maximum down correlation, wherein the reference up chirp has a frequency substantially matching the pilot up chirp, and wherein the reference down chirp has a frequency substantially matching the pilot down chirp; b) producing a timing error by effectively averaging the maximum up correlation and the maximum down correlation; c) producing a frequency error by effectively subtracting the maximum up correlation and the maximum down correlation; and d) synchronizing the receiver to the received signal in accordance with the timing error and the frequency error.

Brief Description of the Drawings

These and other features and advantages of the present invention will become more apparent from a detailed consideration of the invention when taken in conjunction with the drawings in which:

Figure 1 is an example of correlation peaks which may be used by the present invention in order to compute a frequency error between a received signal and a receiver;

Figure 2 is an example of correlation peaks which may be used by the present invention in order to compute a timing error between a received signal and a receiver;

Figure 3 is a schematic diagram of a transmitter and a receiver which provide an exemplary environment for the present invention;

Figure 4 shows the transmitter of Figure 3 in additional detail;

Figure 5 shows the receiver of Figure 3 in additional detail, wherein the receiver includes a synchronizer in accordance with the present invention;

Figure 6 shows the first one hundred samples a reference up chirp that is used by the synchronizer of Figure 5 to synchronize the receiver to the received signal;

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Figures 7 and 9-15 show the synchronizer of Figure 4 in additional detail;

Figure 8 is an example of correlation results produced by the detector of Figure 7; and,

5 Figure 16 illustrates a state diagram for the controller of Figure 7.

Detailed Description

As described below, the present invention involves the synchronization of a receiver to a received signal that contains pilot up and down chirps. As disclosed below, a pilot up chirp (see Figure 6, for example) is a signal whose frequency increases from f_L to f_H according to a predetermined function, and a pilot down chirp is a signal whose frequency decreases from f_H to f_L according to a mirror image of the predetermined function. The receiver of the present invention is arranged to correlate reference up and down chirps to these pilot up and down chirps such that any frequency error between the received signal and the receiver produces correlation peaks on each side of the correlation center as shown by the example in Figure 1, and such that any timing error produces correlation peaks on one side or the other of the correlation center as shown by the example in Figure 2. Then, the frequency error F_E between the received signal and the receiver may be easily computed as proportional to the difference between the frequency correlation peaks, and the timing error T_E between the received signal and the receiver may be easily computed as the average of the timing correlation peaks.

As shown in Figure 3, a communication system 10 implementing this synchronization technique generally includes a transmitter 12 and a receiver 14. The transmitter 12 transmits data over a communication path 16 to the receiver 14. For example, the communication path 16 can be air, space, or cables. To this extent, the transmitter 12 has a signal propagation device 18 such as a modem, an antenna, a satellite dish, or other equipment in order to propagate the data through the communication path 16 to the receiver 14. Similarly, the receiver 14 has a signal acquisition device 20 which acquires the transmitted data from the communication path 16 and provides the acquired data to the receiver 14.

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As shown in Figure 4, the transmitter 12 generally includes a data source 30, a coder 32 which codes the data supplied by the data source 30, a modulator 34 which modulates the coded data onto a carrier, and a filter 36, such as a raised cosine filter, which filters the modulated carrier for supply to the signal propagation device 18. As discussed above, in one exemplary environment of the present invention, the coder 32 may be a coder which receives the data from the data source 30, which selects code vectors in response to the data, and which supplies the code vectors to the modulator 34.

As shown in Figure 5, the receiver 14, in accordance with the present invention, includes a demodulator 40 which receives the data acquired by the signal acquisition device 20 from the communication path 16, which demodulates the acquired data down to baseband, and which supplies the demodulated data to an analog to digital (A/D) convertor 42. The A/D convertor 42 samples the demodulated data at a predetermined sampling rate. (Alternatively, the demodulator 40 and the A/D convertor 42 may be arranged to demodulate the acquired data down to IF, to sample the acquired data at IF, and to demodulate the samples down to baseband.) The samples from the demodulator 40 and the A/D convertor 42 are filtered by a filter 44, such as raised cosine filter, and the filtered samples are supplied to a synchronizer 46, which will be discussed in more detail below. The synchronized data provided by the synchronizer 46 are supplied over a line 46a to an equalizer 48 which reduces intersymbol or interdata interference in the data provided by the synchronizer 46. The synchronizer 46 also supplies an error estimate over a line 46b to the equalizer 48, as will be discussed below. In some cases, the line 46b is two lines, one for a timing error estimate and one for a frequency error estimate. Finally, a decoder 50 decodes the equalized data in order to recover the data which was originally supplied by the data source 30.

In order for the synchronizer 46 to synchronize the receiver 14 to the signal received from the transmitter 12, the transmitter 12 provides a pilot vector in the signal propagated by the signal propagation device 18 over the communication

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path 16 to the signal acquisition device 20. The pilot vector may be a series of alternating pilot up and down chirps which are added by the transmitter 12 to the signal propagated by the signal propagation device 18 to the receiver 14.

The pilot up chirp is essentially defined as $\sin(\omega t^2)$, where the frequency of the pilot up chirp increases according to the function ωt from a minimum at a reference time 0 to a maximum at a time t_N . The pilot down chirp is defined as $\sin(\omega(2t_N - t)^2)$, where the frequency of the pilot down chirp decreases from the maximum at the time reference t_N to the minimum at a time reference $2t_N$. However, these functions for the pilot up and down chirps are exemplary and other functions, such as exponential functions, may be used. The pilot up and down chirps are added continuously to the code vectors transmitted by the transmitter 12 so that the pilot up and down chirps function as a vector pilot. The pilot up and down chirps may be added twelve db down, for example, from the transmitted code vectors.

These up and down chirps are also used in the receiver 14 as reference up and down chirps. By correlating the received signal to the reference up and down chirps, any frequency displacement between the pilot up and down chirps and the reference up and down chirps appears as a time shift between the pilot up and down chirps and the reference up and down chirps. That is, the correlation peak looks as if it is time shifted from the center correlation.

Figure 6 shows the first 100 samples of an exemplary pilot up chirp. The last 100 samples of the pilot down chirp would appear as the negative of the mirror image of the first 100 samples of the pilot up chirp shown in Figure 6. The pilot up chirp and the pilot down chirp are designed to span the entire bandwidth of the transmission. The high frequency components of the pilot up chirp and the pilot down chirp allow fine resolution of position and frequency shifts. Because the pilot up chirp and the pilot down chirp span the entire bandwidth, the synchronizing reference is resistant to narrow band interference and spectral nulls caused by multipath. It should be noted that the waveform shown in Figure 6 is not smooth

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because it is sampled. It should also be noted that the pilot chirp is sinusoidal (as opposed to cosinusoidal) in order to reduce DC bias from the low frequency part of the chirp.

A block diagram of the synchronizer 46 is shown in Figure 7. As discussed above, the pilot up and down chirps are added to the transmitted information data in the transmitter 12. In the communication path 16, the signal propagating through the signal propagation device 18 may encounter various signal impairments such as frequency and phase offset, time delay, multipath, and noise. The pilot up and down chirps permit the synchronizer 46 to synchronize the receiver 14 to the received signal.

The synchronizer 46 includes a detector 60 which correlates the received signal (i.e., the signal received by the receiver 14) with reference up and down chirps having a waveform which substantially matches the waveform of the pilot up and down chirps provided by the transmitter 12 to the information data propagated by the signal propagation device 18. The detector 60 performs this correlation essentially according to the following equation:

$$C(T) = \sum_{t=-L/2}^{L/2} x(t) \cdot y^*(t-T) \quad (1)$$

where L is representative of the length of a chirp and is defined as the number of samples that are taken from an up chirp or a down chirp, the quantity x(t) represents the received pilot up chirp or the received pilot down chirp, as appropriate, the quantity y(t-T) represents the reference up chirp or the reference down chirp, as appropriate, and * represents a complex conjugate function. The factor T in equation (1) is varied from -N to N where N is the number of samples in a chirp. Figure 8 shows an example of the correlations C(T) from -N to N.

Thus, as further discussed below, the correlation is performed over all T, and the correlation point having the largest magnitude is determined. The

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center of the correlation is defined as the correlation point where T is 0. In fact, the quantity $T_{\text{up-peak}}$ represents the value of T at the maximum correlation peak between the received signal and the reference up chirp, and the quantity $T_{\text{down-peak}}$ represents the value of T at the maximum correlation peak between the received
5 signal and the reference down chirp. As discussed below, the frequency error F_E is effectively determined as proportional to the difference between $T_{\text{up-peak}}$ and $T_{\text{down-peak}}$, and the timing error T_E is effectively determined as the average of $T_{\text{up-peak}}$ and $T_{\text{down-peak}}$.

The factor T in equation (1) should vary over the whole up chirp and
10 then over the whole down chirp in order to determine (i) the maximum correlation point $T_{\text{up-peak}}$ between the received signal and the reference up chirp and (ii) the maximum correlation point $T_{\text{down-peak}}$ between the received signal and the reference down chirp. In determining the timing error T_E and the frequency error F_E , M chirps may be used. Thus, in determining $T_{\text{up-peak}}$ and $T_{\text{down-peak}}$, the quantities $T_{\text{up-peak}}$
15 and $T_{\text{down-peak}}$ may each be determined from correlations that are averaged over the M chirps.

The frequency error F_E , the timing error T_E , and a phase error (described below) developed by the detector 60 control a frequency/phase locked
loop 62 and a timing recovery block 64. The output of the frequency/phase locked
20 loop 62 is provided to one input of a multiplier 66. The multiplier 66 multiplies the output from the frequency/phase locked loop 62 and the samples provided by the A/D convertor 42. The output of the multiplier 66 is provided to a delay block 68. The delay block 68 is controlled by the timing recovery block 64 in order to
advance or retard the samples provided by the multiplier 66. Accordingly, the
25 frequency/phase locked loop 62 and the timing recovery block 64 form corresponding control loops which minimize detector error. The output of the delay block 68 is then passed on to the equalizer 48 over the line 46a. The detector 60, the frequency/phase locked loop 62, the timing recovery block 64, and the delay
block 68 are controlled by a controller 70 in accordance with a state diagram
30 described below.

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Generally, the detector 60 is a vector correlator which provides, as outputs, signals proportional to the position of a single correlation peak which is centered when the system is properly synchronized. If the received signal is advanced or delayed, then the correlation peak will be shifted from center. A weighting function may be used to interpolate the points around the peaks to give smooth results.

As described below, the detector 60 implements a fast Fourier transform (FFT) to simplify receiver circuitry and to speed processing. An FFT transforms the received pilot vectors into the frequency domain. The FFT of the received pilot vectors are multiplied by the complex conjugate of the FFT of the reference vectors. The result of this multiplication is transformed back into the time domain by an inverse FFT, and the correlation peak is detected. Using an FFT is particularly advantageous where longer chirps are used because the FFT processes data much faster than does a correlator operating in the time domain.

The detector 60 operates in two different circuit configurations depending upon whether the synchronizer 46 is in lock mode or track mode. A track mode circuit 60a (Figure 9) is used when the detector 60 is operating in track mode. When the detector 60 is operating in lock mode, either a lock mode circuit 60b (Figure 10) or a lock mode circuit 60c (Figures 11 and 12) may be used. The lock mode circuit 60b or 60c controls the frequency/phase lock loop 62 and the timing block 64 in order to lock the receiver 14 onto the received signal based upon differences between the pilot and reference up and down chirps, and the track mode circuit 60a controls the frequency/phase lock loop 62 and the timing block 64 permitting the receiver 14 to thereafter track the timing, frequency, and phase of the received signal, based upon differences between the pilot and reference up and down chirps. The frequency/phase locked loop 62 and the timing recovery block 64 are used with lock parameters for initial lock, and the frequency/phase locked loop 62 and the timing recovery block 64 will be supplied with tracking parameters computed after initial lock for subsequent tracking.

When the synchronizer 46 starts, it goes first into lock mode. Lock mode is used to produce an estimate of frequency and timing errors. As described

below, the negatives of the error estimates are loaded into the frequency/phase locked loop 62 and the timing recovery block 64 as the lock parameters. For example, if the timing error, when computed during lock mode as the average of $T_{\text{up-peak}}$ and $T_{\text{down-peak}}$, is 1, then the lock timing parameter is
5 -1, and if the frequency error, when computed during lock mode as the difference between $T_{\text{up-peak}}$ and $T_{\text{down-peak}}$, is -2, then the lock frequency parameter is 2.

The track mode circuit 60a is shown in Figure 9. The track mode circuit 60a receives the output of the delay block 68 at a window block 120. The window block 120 multiplies the output of the delay block 68 by a window function
10 in order to improve the performance of the FFT. This window function may be chosen to produce a smooth correlation peak. A complex FFT is performed on the output of the window 120 by a CFFT block 122 in order to transform the output of the window block 120 to the frequency domain. A multiplier 124 multiplies the output of the CFFT block 122 by the conjugate of the complex FFT of the reference
15 up chirp. An inverse complex FFT is performed on the product produced by the multiplier 124 at a CFFT^{-1} block 126 in order to transform this product into the time domain. Accordingly, the CFFT block 122, the multiplier 124, and the CFFT^{-1} block 126 form an up chirp correlator. The output of the CFFT^{-1} block 126 is an up correlation vector between the pilot vector and the reference up chirp. This
20 correlation vector is shown generally in Figure 8. A block 128 averages the magnitude of the up correlation vector from the CFFT^{-1} block 126 with previous up correlation vectors in order to enhance the up correlation peak provided by the blocks 122, 124, and 126. It is important to use only the most recent up correlation vectors because the peaks can move as the system adapts. The average is a moving
25 average of the last K up correlation vectors. The up correlation peak is used to adjust frequency and fine timing. This average may alternatively be simply a sum the last K up correlation peaks. The choice of K is a trade off between noise rejection and processing speed, where a larger K means more noise rejection but a slower processing speed.

30 Similarly, a multiplier 130 multiplies the output of the CFFT block 122 by the conjugate of the complex FFT of the reference down chirp. An inverse

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complex FFT is performed on the product produced by the multiplier 130 at a CFFT⁻¹ block 132 in order to transform this product into the time domain. The output of the CFFT⁻¹ block 132 is a down correlation vector between the pilot vector and the reference down chirp. Accordingly, the CFFT block 122, the multiplier 130, and the CFFT⁻¹ block 132 form a down chirp correlator. A block 134 averages the magnitude of the down correlation vector produced by the blocks 122, 130, and 132 with previous down correlation vectors in order to enhance the down correlation peak provided by the blocks 122, 130, and 132 in a manner similar to the block 134.

A peak detector 136 determines the FREQUENCY and TIMING errors from the outputs of the blocks 128 and 134. For example, with respect to the up chirp correlation, the peak detector 136 multiplies the magnitude of the maximum peak by the distance of the maximum peak from the center position of the correlation ($T = 0$). Also, the peak detector 136 multiplies the magnitude of a selected number of points surrounding the maximum peak by their corresponding distances from the center position of the correlation. In performing these multiplications, the sign of the distance is preserved. For example, if a point having a magnitude of 2 is at the position $T = -1$, the multiplication is $(2)(-1) = -2$. These multiplication results are then summed to produce a weighted up correlation peak $T_{up-peak}$. The same process may be applied to the down correlation to produce a weighted down correlation peak $T_{down-peak}$. The peak detector 136 then determines the TIMING error T_E as the average of $T_{up-peak}$ and $T_{down-peak}$ and determines the FREQUENCY error F_E as proportional to the difference between $T_{up-peak}$ and $T_{down-peak}$. This process allows an error signal to be found when a peak is a fractional distance from the center. The TIMING error and FREQUENCY error outputs of the peak detector 136 are passed to the frequency/phase locked loop 62 and the timing recovery block 64. These signals are ghost estimating error signals which are also passed over lines 46b to the equalizer 48 in order to aid operation of the equalizer 48.

The search window used by the peak detector 136 to determine the selected number of points used in calculating the weighted up and down correlation

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peaks may be variable. For example, when the frequency error is low, the search window used in the peak detector 136 may be made smaller. On the other hand, when the frequency error is larger, the search window used in the peak detector 136 may be made larger. This window size adjustment helps to reduce the detection of false peaks when noise is heavy or if there are ghosts present.

A phase detector 138 determines phase errors based upon the output of the multiplier 124 and the output of the multiplier 130. As shown in Figure 9, this phase error determination is performed in the frequency domain, although this phase error determination could be performed in the time domain. In any event, the phase detector 138 measures the phase error of the received signal multiplied by the ideal reference. A phase error for each frequency in the complex FFT of the received signal is determined from the output of the multiplier 124 and from the output of the multiplier 130. Phase is determined using the inverse tangent function. That is, the phase of a frequency is determined according to the following equation:

$$phase = \tan^{-1}\left(\frac{I}{R}\right) \quad (2)$$

where I is the imaginary part of a complex frequency and R is the real part of that complex frequency. An approximation may be used in place of equation (2) in order to simplify the calculation. The phase of each frequency from the multiplier 124 that has a magnitude over a threshold is averaged to give a single up phase error, and the phase of each frequency from the multiplier 132 that has a magnitude over the threshold is averaged to give a single down phase error. Then, the phase detector 138 sums the up and down phase errors in order to produce the overall PHASE error. Following locking of the receiver 14 to the received signal during the lock mode, these TIMING, FREQUENCY, and PHASE errors are used during the tracking mode to maintain the receiver 14 synchronized to the received signal.

The two different lock mode circuits 60b and 60c are shown in Figure 10 and in Figures 11 and 12. If the receiver 14 receives signals from only

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one transmitter 12, or if the receiver 14 receives signals from multiple transmitters 12 which are frequency locked, the lock mode circuit 60b shown in Figure 10 may be used. However, if the receiver 14 receives signals from multiple transmitters 12 which are not locked in frequency, the lock mode circuit 60c shown in Figures 11 and 12 may be used. The reason that the lock mode circuit 60c is used where the receiver 14 receives signals from multiple transmitters 12 that are not locked in frequency is because of the way in which the reference up chirp and reference down chirp correlation vectors are used to find frequency and timing errors. If large ghosts are present, then there will be multiple peaks in the correlation vectors. If the frequencies are locked, the reference up chirp peaks line up in the same order as the reference down chirp peaks. However, if the frequencies are not locked, then the peaks can be in different orders. The lock mode circuit 60c determines which order is appropriate.

In the lock mode circuit 60b shown in Figure 10, the output from the delay block 68 is cross correlated in a cross correlation block 150 with the reference up chirp and is also cross correlated in a cross correlation block 152 with the reference down chirp. The cross correlation block 150 may be similar to the blocks 122, 124, and 126 and the cross correlation block 152 may be similar to the blocks 122, 130, and 132 of Figure 9. The output correlation vectors from the cross correlation block 150 are averaged in an averaging block 154 with corresponding correlation vectors produced by prior correlations. Similarly, the output correlation vectors from the cross correlation block 152 are averaged in an averaging block 156 with corresponding correlation vectors produced by prior correlations. Thus, the averaging blocks 154 and 156 perform a vector average of all previous magnitude vectors. A plurality of correlation peaks may be produced if ghosts are present. The average vectors provided by the averaging blocks 154 and 156 are cross correlated in a block 158. The block 158 also detects the maximum magnitude peak resulting from this cross-correlation and produces a timing shift error T_{FE} proportional to the FREQUENCY error F_E as one-half of the distance of this maximum magnitude peak from the center of the correlation.

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A block 160 shifts the averaged correlation peaks from the averaging block 154 by the timing shift error T_{FE} in one direction and a block 162 shifts the averaged correlation peaks from the averaging block 156 by the timing shift error T_{FE} in the opposite direction in order to shift the separate up and down correlation vectors back to center. The shifted correlation vectors are then added in a summing block 164. The distance from center correlation of the resulting peak having the largest magnitude is determined by a peak detecting block 166 as the TIMING error T_E . The TIMING error output of the peak detector 166 is passed to the timing recovery block 64. This signal is a ghost estimating error signal which is also passed over line 46b to the equalizer 48 in order to aid operation of the equalizer 48.

If multiple signals are received by the receiver 14 from multiple transmitters, the up and down correlation peaks must be matched up so frequencies and timing can be calculated. All possible combinations of peaks should be used to calculate the FREQUENCY and TIMING errors by adding and subtracting distances of peaks from center. The negatives of these FREQUENCY and TIMING errors are used as correction parameters in order to adjust the frequency/phase locked loop 62 and the timing recovery block 64. Alternatively, the correction parameters may be used to create multiple correlation reference vectors.

Accordingly, the lock mode circuit 60c operates in two modes. First, in a detect mode shown in Figure 11, the up and down chirp correlations are performed by blocks 180-188 in the same or similar fashion as they are performed by the blocks 122, 124, 126, 130, and 132 of Figure 9. The correlation peaks are averaged in blocks 190 and 192 and are peak detected in a block 194. The peak detection block 194 then provides the TIMING and FREQUENCY errors T_E and F_E . The TIMING error and FREQUENCY error outputs of the peak detection block 194 are passed to the frequency/phase locked loop 62 and the timing recovery block 64. As discussed above, these signals are ghost estimating error signals which are also passed over lines 46b to the equalizer 48 in order to aid operation of the equalizer 48.

The peak detection block 194 provides the TIMING and FREQUENCY errors T_E and F_E according to the following operation. Let it be assumed that the up and down correlations being output by the averaging blocks 190 and 192 each have two main peaks, peaks $T_{up-peak-A}$ and $T_{down-peak-A}$ representing the main received signal and peaks $T_{up-peak-B}$ and $T_{down-peak-B}$ representing a ghost of the main received signal. Based upon these peaks, the peak detector 194 then determines four sets of TIMING and FREQUENCY errors T_{EAA} and F_{EAA} , T_{EBB} and F_{EBB} , T_{EAB} and F_{EAB} , and T_{EBA} and F_{EBA} . For example, the peak detector 194 determines the TIMING error T_{EAA} as the average of $T_{up-peak-A}$ and $T_{down-peak-A}$, and determines the FREQUENCY error F_{EAA} as proportional to the difference between $T_{up-peak-A}$ and $T_{down-peak-A}$; the peak detector 194 determines the TIMING error T_{EBB} as the average of $T_{up-peak-B}$ and $T_{down-peak-B}$, and determines the FREQUENCY error F_{EBB} as proportional to the difference between $T_{up-peak-B}$ and $T_{down-peak-B}$; the peak detector 194 determines the TIMING error T_{EAB} as the average of $T_{up-peak-A}$ and $T_{down-peak-B}$, and determines the FREQUENCY error F_{EAB} as proportional to the difference between $T_{up-peak-A}$ and $T_{down-peak-B}$; and, the peak detector 194 determines the TIMING error T_{EBA} as the average of $T_{up-peak-B}$ and $T_{down-peak-A}$, and determines the FREQUENCY error F_{EBA} as proportional to the difference between $T_{up-peak-B}$ and $T_{down-peak-A}$.

The four sets of TIMING and FREQUENCY errors T_{EAA} and F_{EAA} , T_{EBB} and F_{EBB} , T_{EAB} and F_{EAB} , and T_{EBA} and F_{EBA} are used to adjust the references PRSA REF, PRSB REF, PRSC REF, and PRSD REF supplied to a verify mode portion (Figure 12) of the lock mode circuit 60c. These references can be pseudo-random sequence (PRS) vectors which have the advantage that a frequency error does not look like a time shift so that a good match results in a center peak having a large magnitude. The references PRSA REF, PRSB REF, PRSC REF, and PRSD REF may all be identical before adjustment. Specifically, TIMING and FREQUENCY errors T_{EAA} and F_{EAA} are used to adjust the reference PRSA REF; the TIMING and FREQUENCY errors T_{EBB} and F_{EBB} are used to adjust the reference PRSB REF; the TIMING and FREQUENCY errors T_{EAB} and F_{EAB} are used to adjust the reference PRSC REF; and, the TIMING and FREQUENCY

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errors T_{EBA} and F_{EBA} are used to adjust the reference PRSD REF. For example, the reference PRSA REF, which is the complex conjugate of the FFT of a reference vector A, is integer time shifted and fractionally filtered by the TIMING error T_{EAA} and is multiplied by a function of the FREQUENCY error F_{EAA} in a manner similar to that described below in connection with Figures 13 and 15. This function could be a cosine function, an exponential function, or the like. Accordingly, the references compensate for the timing and frequency of each possible match.

The received signal is then correlated with these adjusted references PRSA REF, PRSB REF, PRSC REF, and PRSD REF, and the results for all combinations of references are compared. The negatives of the TIMING and FREQUENCY errors are passed to the frequency/phase locked loop 62 and the timing recovery block 64 as the correction parameters. The best correlation results are the results having the largest amplitude peaks and having correlation peaks that are closest to center correlation. If none of the combinations produce good correlation peaks, the lock process starts over.

Thus, the correlators of Figure 12 have a common CFFT block 200. A multiplier 202 multiplies the output of the CFFT block 200 by the PRSA reference, a multiplier 204 multiplies the output of the CFFT block 200 by a PRSB reference, a multiplier 206 multiplies the output of the CFFT block 200 by a PRSC reference, and a multiplier 208 multiplies the output of the CFFT block 200 by a PRSD reference. The outputs of the multipliers 202-208 are inverse complex fast Fourier transformed in corresponding $CFFT^{-1}$ blocks 210, 212, 214, and 216. Averaging blocks 218, 220, 222, and 224 compute running averages in a fashion previously described. Peak detectors 226 then detect the largest magnitude up and down peaks from the corresponding average blocks 218, 220, 222, and 224. A best peak selection block 228 determines the best correlation results by determining which set of up and down peaks (i) have the largest amplitude and (ii) are closest to center correlation. The best peak selection block also computes the TIMING and FREQUENCY errors based upon the best correlation results. The TIMING error and FREQUENCY error outputs are passed to the frequency/phase locked loop 62 and the timing recovery block 64. These signals are ghost estimating error signals

which are also passed over lines 46b to the equalizer 48 in order to aid operation of the equalizer 48.

The timing block 64 is shown in Figure 13. After the lock mode is completed, the negative of the timing error T_E from the peak detector 166 or 228, as appropriate, is loaded as a correction parameter into an accumulator 302. This timing error correction parameter in the accumulator 302 adjusts the delay block 68 in one step in order to center the received signal in the middle of its tracking detectors. When the received signal is centered in the middle of its tracking detectors, the signal and reference block boundaries are aligned and the correlation peak is at a maximum.

When the system is tracking, the timing error T_E from the peak detector 136 is input to a low pass filter 304 of the timing block 64. During tracking, the accumulator 302 and the low pass filter 304 perform a continuous timing adjustment by selecting an integer amount of delay in the delay block 68 and by changing tap values of a fractional delay filter of the delay block 68. This timing correction uses a loop comprising the delay block 68, the detector 60, and the timing block 64, where the timing block 64 comprises the low pass filter 304 and the timing accumulator 302 which is analogous to a frequency oscillator, (i.e., $1/s$). The response of the low pass filter 304 is given by the following equations:

$$F(s) = \frac{1}{1 + \tau s} \quad (3)$$

$$\tau = \frac{1}{2\pi f_c} \quad (4)$$

The quantity f_c in equation (4) is the cut off frequency of the low pass filter 304. The closed loop response of the loop containing the delay block 68, the detector 60, and the timing block 64 is given by the following equation:

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$$H(s) = \frac{k \cdot F(s)}{(s + k \cdot F(s))} = \frac{k}{\tau \cdot s^2 + s + k} \quad (5)$$

where k is the gain of the loop. Given a desired loop bandwidth and damping factor, the gain k and the low pass filter cut-off frequency f_c can be calculated. The timing block 64 functions at a rate f_s/N , where f_s is the system sampling frequency, and N is the vector chirp length. This loop can run at this slower rate because timing changes slowly. (Equation (5) is an approximation of the loop equation derived from simplifications of the actual response.)

The delay imposed by the timing block 64 is some integer number of samples and a fraction of a sample. That is, when the timing error T_E is determined in the detector 60, the timing error T_E typically involves an integer part plus a fractional part. As shown in Figure 14, the integer part is used to control a multiplexer 310 that selects an appropriate number of delay registers 312 in order to advance or retard the samples by the integer part. The fractional part is used to change the tap values of a fractional delay filter 314, as discussed above, so that the samples are advanced or retarded by a fraction of a sample as determined by the fractional part. The fractional delay filter 314 can use linear, cubic-spline, piecewise parabolic, nth-order polynomial, or other interpolation. As a further alternative, a FIR filter may be used. If a FIR filter is used, the taps of the FIR filter are adjusted according to the fractional part of the timing output of the timing block 64.

The frequency/phase lock loop 62 is shown in additional detail in Figure 15. The frequency/phase lock loop 62 includes a frequency correction portion and a phase correction portion. After the lock mode is completed, the negative of the frequency error F_E from the peak detector 166 or 228, as appropriate, is loaded into a gain and filter block 350. This frequency error correction parameter in the gain and filter block 350 is used by the frequency/phase lock loop 62 and the multiplier 66 to eliminate any frequency error between the reference pilot and the receiver 14.

During tracking, the frequency error F_E provided by the peak detector 136 is supplied to the gain and filter block 350. The gain and filter block 350

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applies gain to the frequency error and then implements a first order Butterworth low pass filter. (The negative of the FREQUENCY error determined during the lock mode is supplied to the feedback output of the Butterworth low pass filter.) Ignoring the phase loop, the gain and filter block 350 comprise the frequency lock loop. The frequency/phase lock loop 62. The response of the Butterworth low pass filter is given by the following equation:

$$F(s) = \frac{1}{1 + \tau s} \quad (6)$$

$$\tau = \frac{1}{2\pi f_c} \quad (7)$$

where the quantity f_c is the cut-off frequency of the Butterworth low pass filter. The closed loop response of the loop containing the multiplier 66, the delay block 68, the detector 60, the gain and filter block 350, a voltage controlled oscillator 352 (described below), and a multiplier 354 (also described below) is given by the following equation:

$$H(s) = \frac{k \cdot F(s)}{1 + k \cdot F(s)} = \frac{k \tau^2}{\tau s + k + 1} \quad (8)$$

where k is loop gain. By adjusting τ , the noise bandwidth is affected, and by adjusting the gain k , the noise bandwidth and residual error frequency are affected. Additionally, the frequency detector operates at the rate of f_s/N , where f_s is the system sampling frequency, and N is the vector chirp length, as discussed above. The low pass filter of the gain and filter block 350 operates at the full sampling rate f_s to give smoother output. A zero-order-hold may be used to match the sampling rates. Averaging of the correlations is done, as indicated above, in order to reduce noise.

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The output of the gain and filter block 350 controls a voltage controlled oscillator 352 whose output is provided to a multiplier 354. The multiplier 354 multiplies the output of the voltage controlled oscillator 352 by the output of a gain and filter block 360. (Equation (8) is an approximation of the loop equation derived from simplifications of the actual response.)

The output from the phase detector 138 is provided to the gain and filter block 360. The gain and filter block 360 imposes a gain on the signal from the phase detector 138 and then filters the resulting signal using a first order active low pass filter. This type of filter gives a large gain at DC in order to allow the phase lock loop portion of the frequency/phase lock loop 62 to lock with low phase error, while giving noise rejection. Accordingly, if the frequency loop of the frequency/phase lock loop 62 is ignored, the phase loop is a second order phase lock loop. The transfer function of the low pass filter is given by the following equation:

$$F(s) = \frac{1 + \tau s}{s} \quad (9)$$

and the closed loop response of the phase loop containing the multiplier 66, the delay block 68, the detector 60, the gain and filter block 360, and the multiplier 354 is given by the following equation:

$$H(s) = \frac{k \cdot F(s)}{s + k \cdot F(s)} = \frac{k \cdot \tau \cdot s + k}{s^2 + k \cdot \tau \cdot s + k} \quad (10)$$

Given a desired loop bandwidth and damping factor, the gain and low pass filter cut-off of the gain and filter block 360 can be calculated. The phase detector 138 may be operated at the rate of f_s/N because phase changes slowly. The output of the gain and filter block 360 is applied to the multiplier 354. The multiplier 354 multiplies

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the output from the voltage controlled oscillator 352 by the output from the gain and filter block 360. Then, the multiplier 66 multiplies the output from the multiplier 354 by the samples from the A/D convertor 42.

The controller 70 of Figure 7 operates in accordance with the state diagram of Figure 16. At start, when operation of the receiver 14 is first initiated or when sync is lost such as due to a channel change, the controller 70 first enters the lock mode by controlling an appropriate one of the lock mode circuits 60b and 60c, depending on whether the receiver receives signals from only one transmitter, or from multiple transmitters which are frequency locked, or from multiple transmitters which are not locked in frequency. If the controller 70 enters the lock mode by controlling the lock mode circuit 60b, and once lock is complete, the controller 70 enters the track mode by appropriate control of the track mode circuit 60a. On the other hand, if the controller 70 enters the lock mode by controlling the lock mode circuit 60c, the controller 70 controls the lock mode portion of the lock mode circuit 60c until the appropriate timing and frequency errors are calculated, and then enters the verify mode by controlling the verify portion of the lock mode circuit 60c until lock is verified. Thereafter, the controller 70 enters the track mode by appropriate control of the track mode circuit 60a. Once in the track mode, the controller 70 can return to the lock mode if sync is lost.

Certain modifications of the present invention have been discussed above. Other modifications will occur to those practicing in the art of the present invention. For example, the invention described above is particularly useful in vestigial sideband (VAB) or single sideband (SSB) systems. However, in a modified form, the invention described above may be used in double sideband (DSB) or quadrature amplitude modulated (QAM) systems.

Accordingly, the description of the present invention is to be construed as illustrative only and is for the purpose of teaching those skilled in the art the best mode of carrying out the invention. The details may be varied substantially without departing from the spirit of the invention, and the exclusive use of all modifications which are within the scope of the appended claims is reserved.

WHAT IS CLAIMED IS:

1. A receiver, wherein the receiver receives a received signal containing a pilot synchronizing signal, wherein the receiver includes a detector arranged to correlate the received signal with a reference synchronizing signal, wherein the reference synchronizing signal corresponds to the pilot synchronizing signal, and wherein the receiver includes a signal adjuster arranged to synchronize the receiver to the received signal in response to the correlation performed by the detector, the receiver being CHARACTERIZED IN THAT:

the pilot synchronizing signal comprises a pilot up chirp and a pilot down chirp,

the reference synchronizing signal comprises a reference up chirp and a reference down chirp,

the reference up chirp corresponds to the pilot up chirp, and

the reference down chirp corresponds to the pilot down chirp.

2. The receiver of claim 1 wherein the pilot up chirp has an increasing frequency, wherein the pilot down chirp has a decreasing frequency, wherein the reference up chirp has an increasing frequency substantially matching the pilot up chirp, and wherein the reference down chirp has a decreasing frequency substantially matching the pilot down chirp.

3. The receiver of claim 2 wherein the frequency of the pilot up chirp increases from a time reference zero to a time reference t_N , and wherein the frequency of the pilot down chirp decreases from the time reference t_N to a time reference $2t_N$.

4. The receiver of claim 2 wherein the detector is arranged to produce a maximum up correlation between the received signal and the reference up chirp, wherein the detector is arranged to produce a maximum down correlation between the received signal and the reference down chirp, wherein the detector is arranged to produce a frequency error by effectively subtracting the maximum up correlation and the maximum down correlation, and wherein the signal adjuster is arranged to synchronize to the received signal in accordance with the frequency error.

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5 5. The receiver of claim 2 wherein the detector is arranged to produce a maximum up correlation between the received signal and the reference up chirp, wherein the detector is arranged to produce a maximum down correlation between the received signal and the reference down chirp, wherein the detector is arranged to produce a timing error by effectively averaging the maximum up correlation and the maximum down correlation, and wherein the signal adjuster is arranged to synchronize to the received signal in accordance with the timing error.

10 6. The receiver of claim 5 wherein the detector is arranged to produce a frequency error by effectively subtracting the maximum up correlation and the maximum down correlation, and wherein the signal adjuster is arranged to synchronize to the received signal in accordance with the frequency error.

15 7. The receiver of claim 6 wherein the signal adjuster comprises a multiplier and a delay, wherein the multiplier multiplies the received signal and a frequency correction based upon the frequency error, and wherein the delay advances or retards, as appropriate, a result of the multiplier in response to a timing correction based upon the timing error.

20 8. The receiver of claim 1 wherein the detector is arranged to produce a maximum up correlation between the received signal and the reference up chirp, wherein the detector is arranged to produce a maximum down correlation between the received signal and the reference down chirp, wherein the detector is arranged to produce a frequency error by effectively subtracting the maximum up correlation and the maximum down correlation, and wherein the signal adjuster is arranged to synchronize to the received signal in accordance with the frequency error.

25 9. The receiver of claim 1 wherein the detector is arranged to produce a maximum up correlation between the received signal and the reference up chirp, wherein the detector is arranged to produce a maximum down correlation between the received signal and the reference down chirp, wherein the detector is arranged to produce a timing error by effectively averaging the maximum up correlation and the maximum down correlation, and wherein the signal adjuster is arranged to synchronize to the received signal in accordance with the timing error.

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10. The receiver of claim 9 wherein the detector is arranged to produce a maximum up correlation between the received signal and the reference up chirp, wherein the detector is arranged to produce a maximum down correlation between the received signal and the reference down chirp, wherein the detector is
5 arranged to produce a frequency error by effectively subtracting the maximum up correlation and the maximum down correlation, and wherein the signal adjuster is arranged to synchronize to the received signal in accordance with the frequency error.

11. The receiver of claim 10 wherein the detector is arranged to
10 produce a frequency error by effectively subtracting the maximum up correlation and the maximum down correlation, and wherein the signal adjuster is arranged to synchronize to the received signal in accordance with the frequency error.

12. The receiver of claim 11 wherein the signal adjuster comprises a multiplier and a delay, wherein the multiplier multiplies the received signal and a
15 frequency correction based upon the frequency error, and wherein the delay advances or retards, as appropriate, a result of the multiplier in response to a timing correction based upon the timing error.

13. The receiver of claim 1 wherein the detector comprises a sampler arranged to sample the received signal in order to produce received signal samples,
20 wherein the detector is arranged to correlate the resulting received signal samples with the reference up chirp and the reference down chirp, wherein the pilot up chirp has an increasing frequency, wherein the pilot down chirp has a decreasing frequency, wherein the reference up chirp has an increasing frequency substantially matching the pilot up chirp, wherein the reference down chirp has a decreasing
25 frequency substantially matching the pilot down chirp, and wherein the signal adjuster synchronizes the receiver to the received signal samples.

14. The receiver of claim 13 wherein the detector is arranged to produce a maximum up correlation between the received signal samples and the reference up chirp, wherein the detector is arranged to produce a maximum down
30 correlation between the received signal samples and the reference down chirp, wherein the detector is arranged to produce a frequency error by effectively

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subtracting the maximum up correlation and the maximum down correlation, and wherein the signal adjuster is arranged to adjust the received signal samples in accordance with the frequency error.

5 15. The receiver of claim 13 wherein the detector is arranged to produce a maximum up correlation between the received signal samples and the reference up chirp, wherein the detector is arranged to produce a maximum down correlation between the received signal samples and the reference down chirp, wherein the detector is arranged to produce a timing error by effectively averaging the maximum up correlation and the maximum down correlation, and wherein the
10 signal adjuster is arranged to adjust the received signal samples in accordance with the timing error.

16. The receiver of claim 15 wherein the detector is arranged to produce a frequency error by effectively subtracting the maximum up correlation and the maximum down correlation, and wherein the signal adjuster is arranged to adjust
15 the received signal samples in accordance with the frequency error.

17. The receiver of claim 16 wherein the signal adjuster comprises a multiplier and a delay, wherein the multiplier multiplies the received signal samples and a frequency correction based upon the frequency error, and wherein the delay advances or retards, as appropriate, a result of the multiplier in response to a timing
20 correction based upon the timing error.

18. The receiver of claim 1 wherein the detector is arranged to detect a frequency error by correlating the received signal with the reference up chirp and the reference down chirp, and wherein the signal adjuster is arranged to correct the frequency error in accordance with the following equations:

$$F(s) = \frac{1}{1 + \tau s}$$

$$\tau = \frac{1}{2\pi f_c}$$

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$$H(s) = \frac{k \cdot F(s)}{1 + k \cdot F(s)} = \frac{k\tau^2}{\tau s + k + 1}$$

where f_c is a cut-off frequency and k is loop gain.

- 5 19. The receiver of claim 1 wherein the detector is arranged to detect a timing error by correlating the received signal with the reference up chirp and the reference down chirp, and wherein the signal adjuster is arranged to correct the timing error in accordance with the following equations:

$$F(s) = \frac{1}{1 + \tau s}$$

$$\tau = \frac{1}{2\pi f_c}$$

$$H(s) = \frac{k \cdot F(s)}{(s + k \cdot F(s))} = \frac{k}{\tau \cdot s^2 + s + k}$$

where f_c is a cut-off frequency and where k is the gain.

- 10 20. The receiver of claim 19 wherein the detector is arranged to detect a frequency error by correlating the received signal with the reference up chirp and the reference down chirp, and wherein the signal adjuster is arranged to correct the frequency error in accordance with the following equations:

15

$$F(s) = \frac{1}{1 + \tau s}$$

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where f_c is a cut-off frequency and k is loop gain.

$$\tau = \frac{1}{2\pi f_c}$$

$$H(s) = \frac{k \cdot F(s)}{1 + k \cdot F(s)} = \frac{k\tau^2}{\tau s^2 + k + 1}$$

21. The receiver of claim 20 wherein the detector further comprises a phase error detector arranged to detect a phase error between the received signal and the reference up and down chirps and to produce a phase correction based upon the phase error, wherein the signal adjuster comprises first and second multipliers, wherein the first multiplier multiplies the frequency correction and the phase correction to produce a multiplication result, wherein the second multiplier multiplies the multiplication result by the received signal, and wherein the phase error detector operates in accordance with the following equations:

$$F(s) = \frac{1 + \tau s}{s}$$

$$H(s) = \frac{k \cdot F(s)}{s + k \cdot F(s)} = \frac{k \cdot \tau \cdot s + k}{s^2 + k \cdot \tau \cdot s + k}$$

where f_c is a cut-off frequency of the phase error detector and k is loop gain.

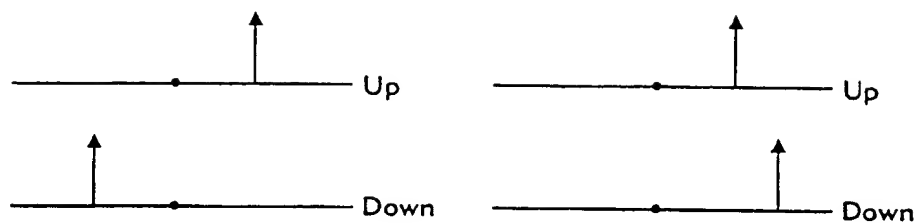
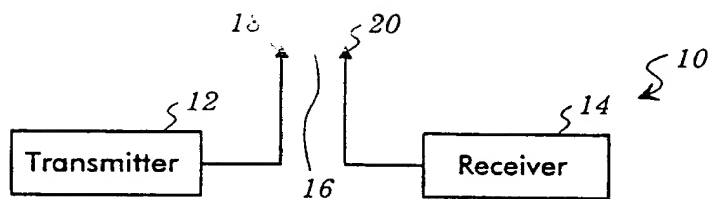
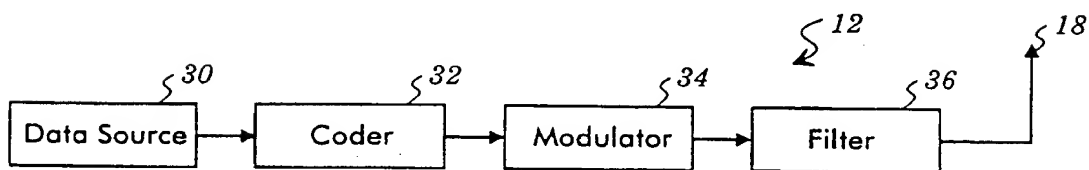
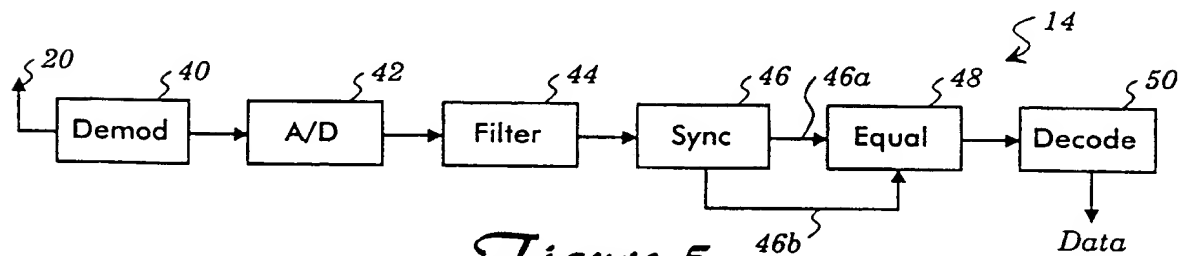
22. The receiver of claim 1 wherein the detector produces a timing error and a frequency error by correlating the received signal with the reference up chirp and the reference down chirp, and wherein the signal adjuster synchronizing the receiver to the received signal in accordance with the timing error and the frequency error.

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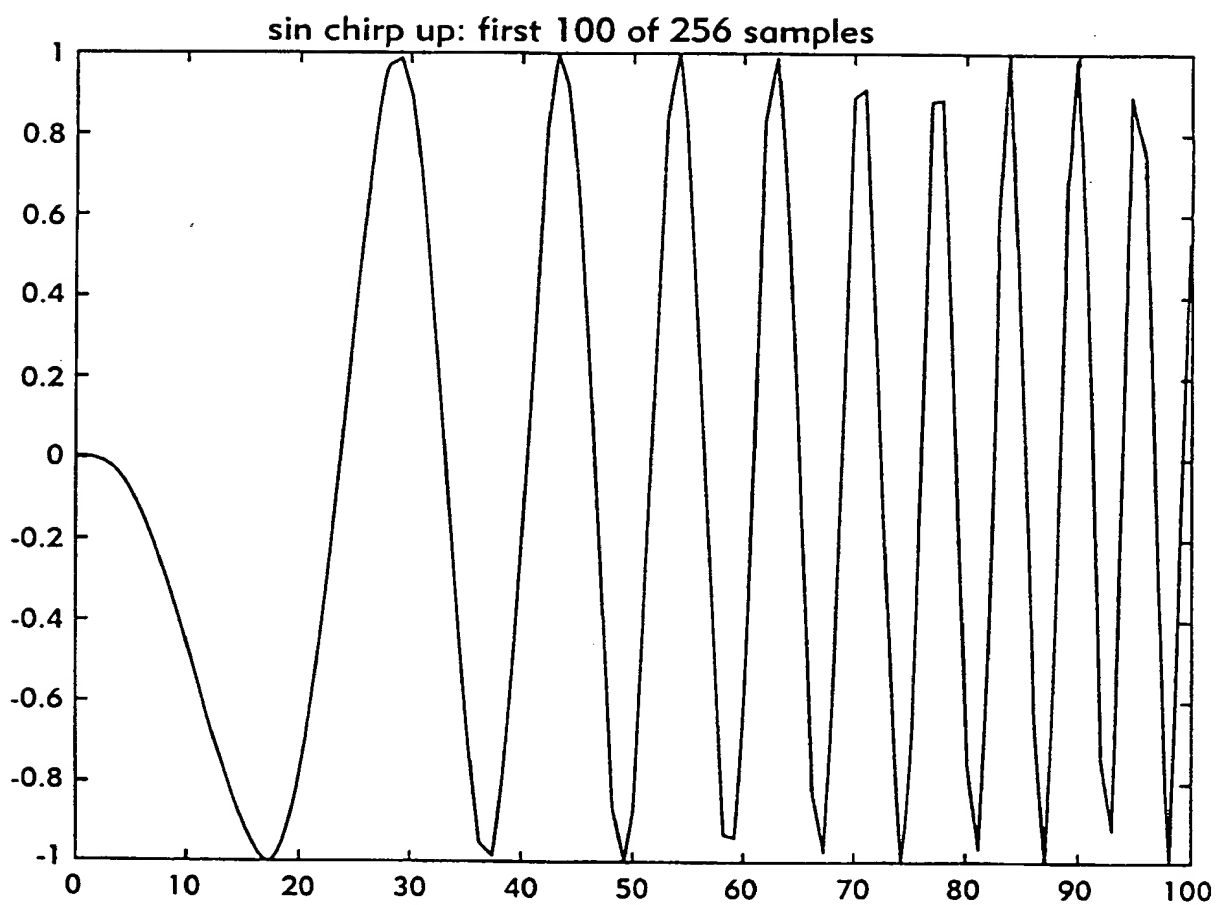
23. The receiver of claim 22 wherein the signal adjuster multiplies the received signal and a frequency correction based upon the frequency error, and advances or retards, as appropriate, a result of the multiplication by a timing correction based upon the timing error.

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*Figure 1**Figure 2**Figure 3**Figure 4**Figure 5*

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*Figure 6*

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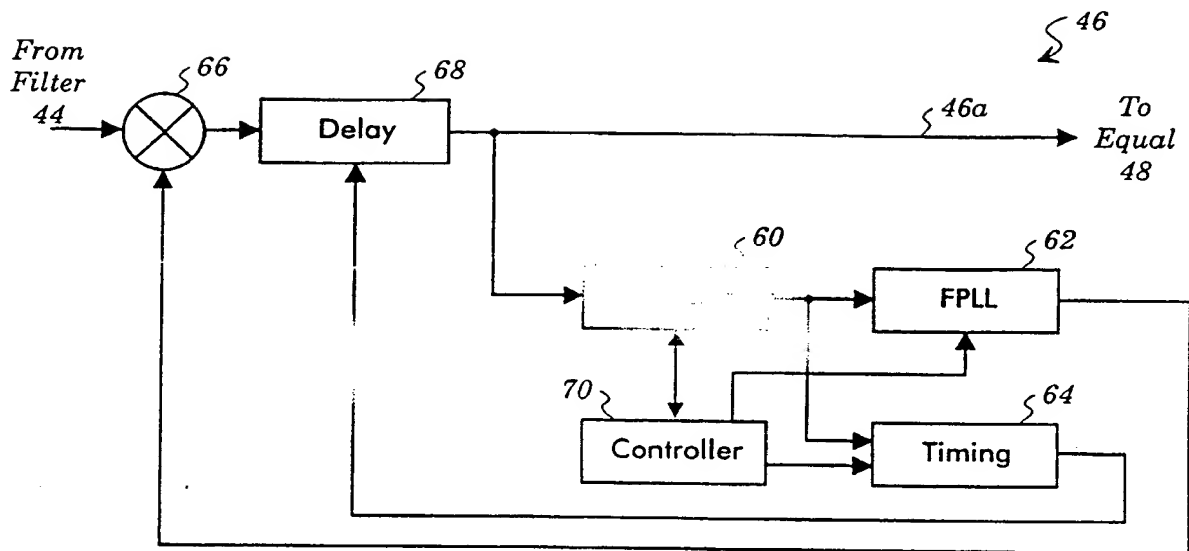


Figure 7

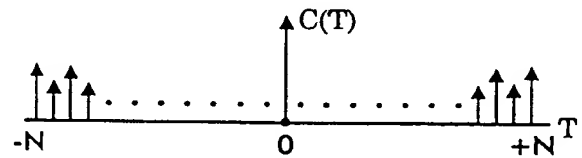


Figure 8

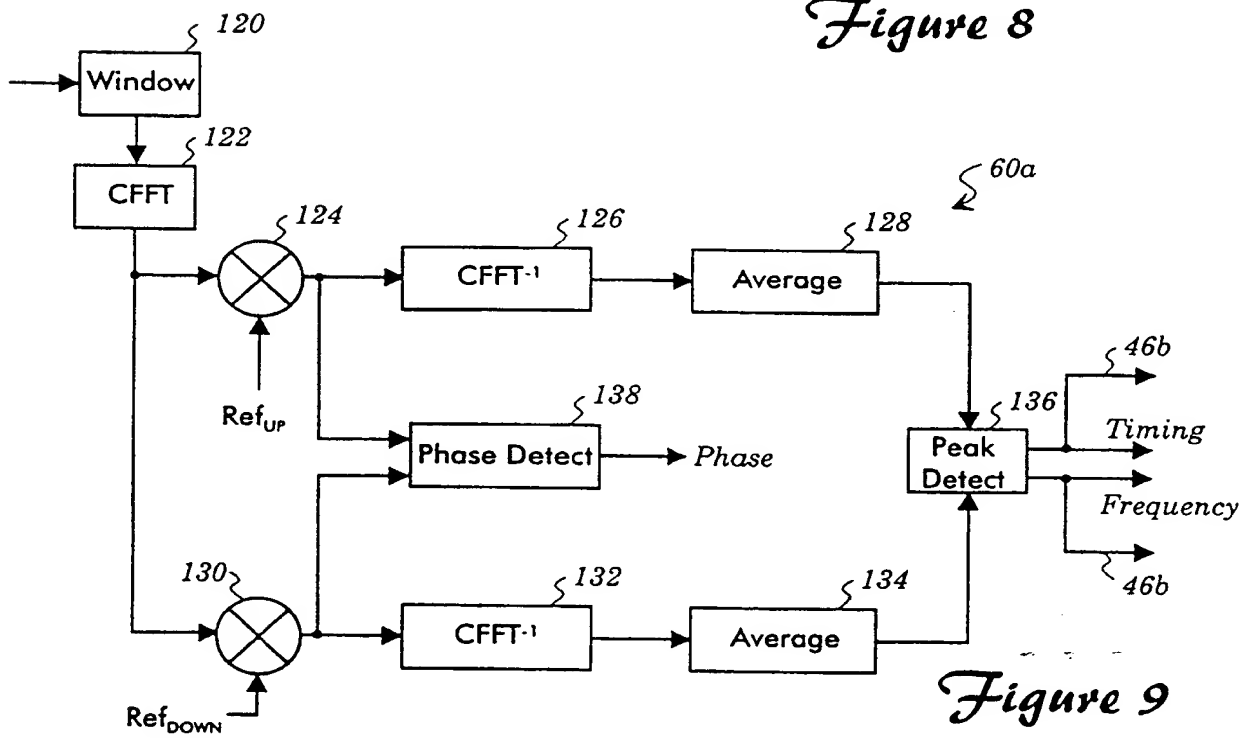


Figure 9

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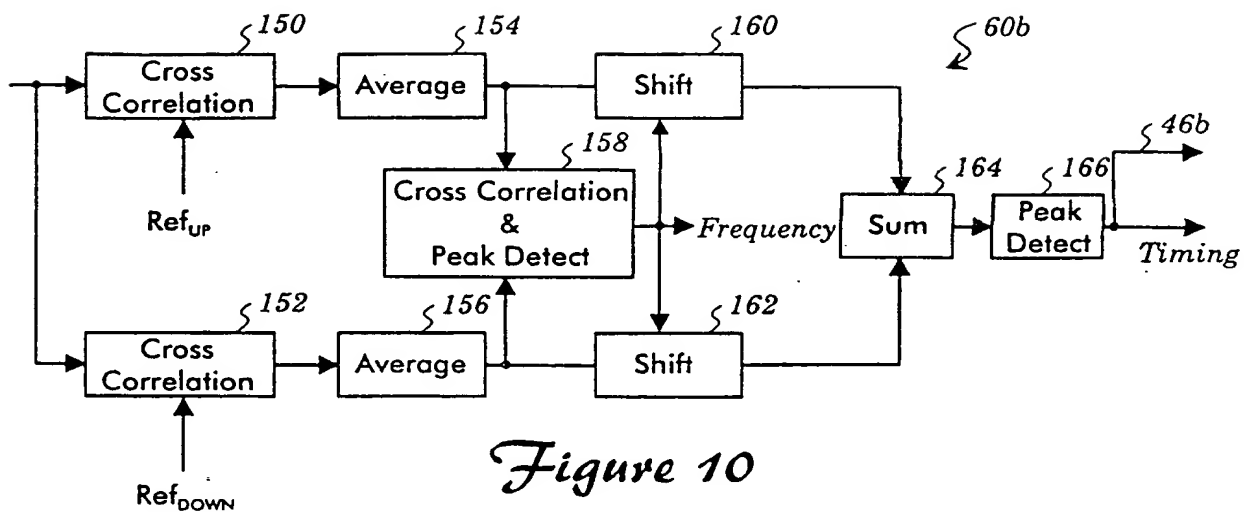


Figure 10

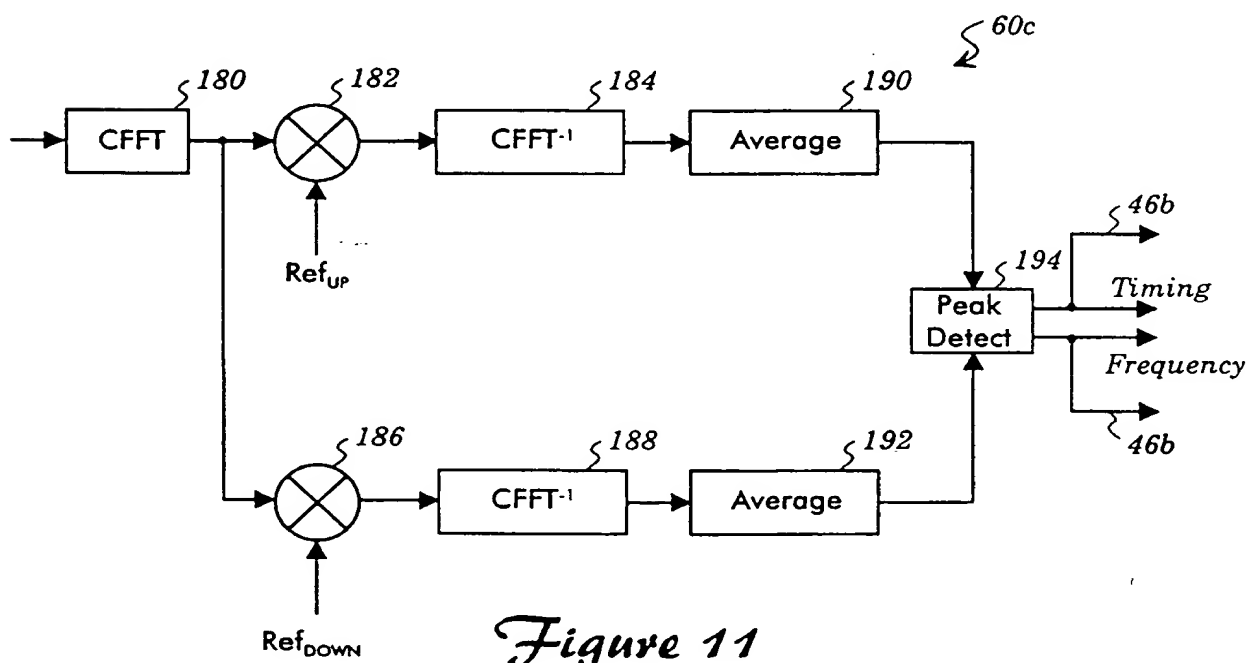


Figure 11

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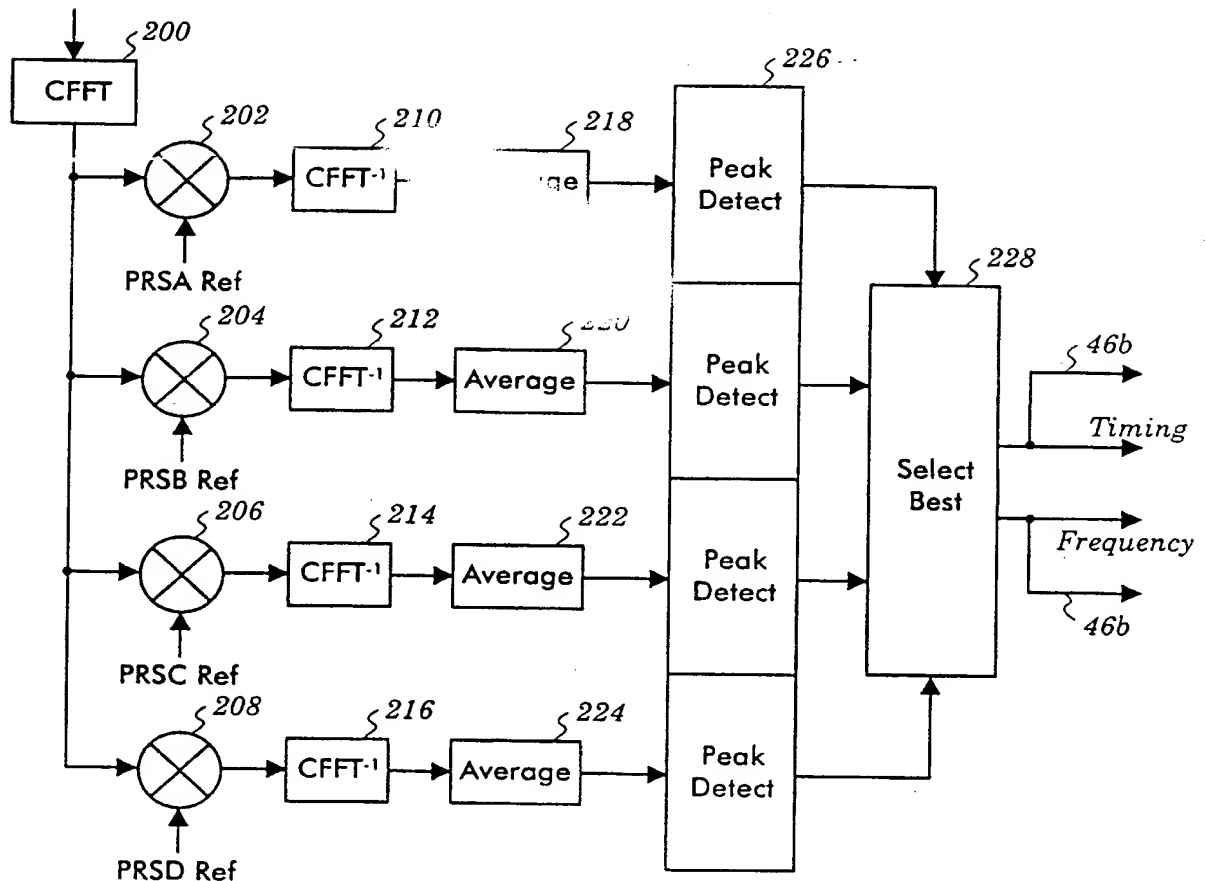


Figure 12

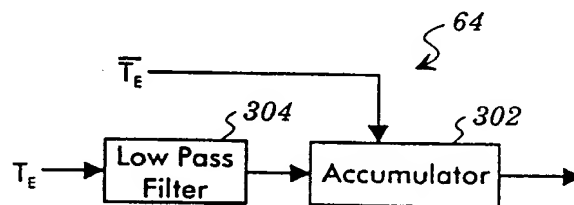


Figure 13

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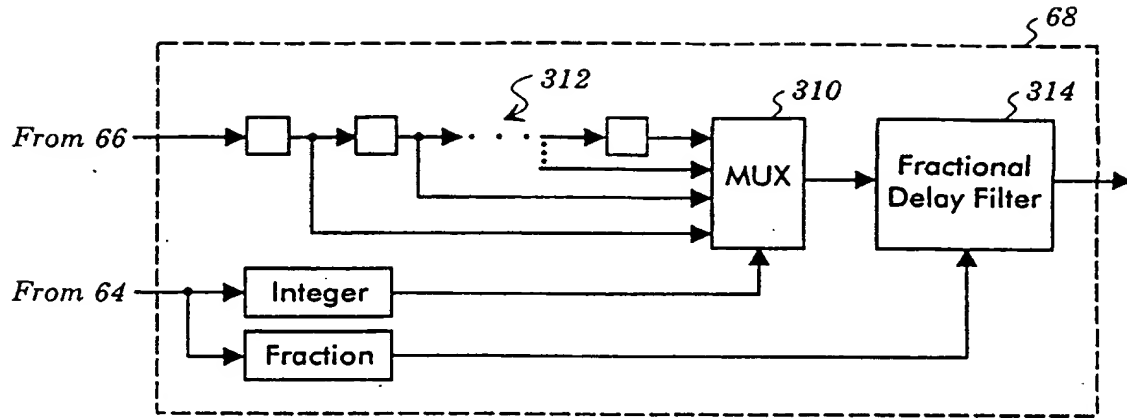


Figure 14

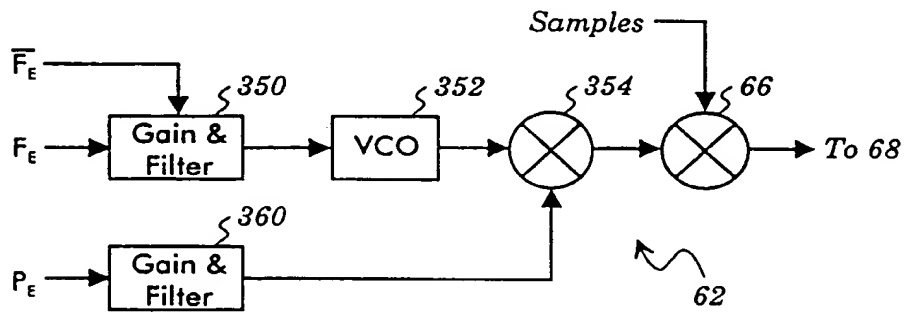


Figure 15

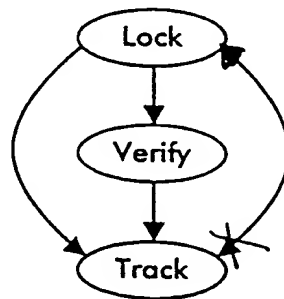


Figure 16

INTERNATIONAL SEARCH REPORT

International Application No

PCT/US 99/05303

A. CLASSIFICATION OF SUBJECT MATTER
IPC 6 H04B1/69

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC 6 H04B H04L H04J

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	<p>WO 96 02990 A (LOENROTH BRIAN ;RINGSET VIDAR (NO); HD DIVINE (SE); ROTH GOERAN (S) 1 February 1996 see page 4, line 35 - page 5, line 37 see page 6, line 28 - page 7, line 3 see page 8, line 6 - line 11 see page 8, line 16 - line 28 see page 9, line 5 - page 10, line 3 see page 10, line 21 - line 27 see page 10, line 31 - page 11, line 13</p> <p style="text-align: center;">--- -/-</p>	<p>1,2,4-6, 8-11, 13-16,22</p>

☒ Further documents are listed in the continuation of box C.

☒ Patent family members are listed in annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

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INTERNATIONAL SEARCH REPORT

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C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

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X	<p>WO 96 19056 A (LOENROTH BRIAN ;RINGSET VIDAR (NO); HD DIVINE (SE); ROTH GOERAN (S) 20 June 1996 See abstract see page 3, line 26 - page 4, line 22 see page 5, line 34 - page 7, line 20 see page 7, line 29 - page 8, line 4 see figures 1,2</p>	<p>1,2,4,8, 13,14,22</p>
A	<p>US 5 278 862 A (VANDER MEY) 11 January 1994 see column 1, line 40 - column 2, line 22 see column 3, line 35 - line 46; claim 1; figure 1B</p>	<p>1</p>
A	<p>US 5 410 621 A (HYATT) 25 April 1995 see column 38, line 14 - line 41 see column 118, line 54 - line 57 see column 123, line 51 - column 124, line 32 see column 135, line 27 - column 136, line 13 see figures 1C,1D,1E,1F see figures 7C,7E,7F</p>	<p>1</p>

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